

Appl. No. 10/620,743
Examiner: KENNEDY, JENNIFER M, Art Unit 2812
In response to the Office Action dated November 29, 2004

Date: February 22, 2005
Attorney Docket No. 10112491

AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph at page 4, line 8 with the following rewritten paragraph:

— Accordingly, the present invention provides a method for forming a trench capacitor. A semiconductor substrate is provided, a deep trench and a deep trench capacitor are formed therein, the deep trench capacitor having a node dielectric layer and a storage node, the node dielectric layer formed covering a sidewall and a bottom portion between the deep trench and the storage node of the deep trench capacitor, and the storage node filling the deep trench to a predetermined depth. The deep trench top portion is ion implanted ~~[[to]]~~ at a predetermined angle to form an ion doped area on a single sidewall of the semiconductor substrate and the top surface of the deep trench capacitor. ~~The semiconductor substrate is oxidized to form an An~~ oxide layer is formed on the ion doped area. A sidewall layer is formed ~~on the exposed semiconductor substrate~~ on the sidewall of the deep trench using the oxide layer as a mask, wherein the sidewall layer is isolated from the storage node of the deep trench capacitor. The oxide layer is removed. A barrier layer is formed on the sidewall interior of the deep trench and the sidewall layer. The deep trench is filled with a conducting layer.

Please replace the paragraph at page 4, line 25 with the following rewritten paragraph:

— Accordingly, the present invention provides another method for forming a trench capacitor. A semiconductor substrate is provided, with a deep trench and a deep trench capacitor formed therein, the deep trench capacitor having a node dielectric layer and a storage node, the node dielectric layer covering a sidewall and a bottom portion between the deep trench and the storage node of the deep trench capacitor, the storage node filling the deep trench to a predetermined depth, wherein the deep trench has a first sidewall and a second sidewall. The deep trench top portion is ion implanted ~~[[to]]~~ at a predetermined angle to form an ion doped area on the semiconductor substrate of the first sidewall and the top surface of the deep trench capacitor. The semiconductor substrate is oxidized to form a first oxide layer on the ion doped area and a second oxide layer on the second sidewall, wherein the thickness of the first oxide layer exceeds the thickness of the second oxide layer. The second oxide layer is removed to expose the semiconductor substrate of the second sidewall of the deep trench. A sidewall layer is formed on the second sidewall using the first oxide layer as a mask. The first

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oxide layer is removed to expose the semiconductor substrate of the first sidewall. A first barrier layer is conformally formed on the first sidewall, the sidewall layer, and the deep capacitor. Spacers are formed on the first sidewall and a sidewall of the sidewall layer sequentially. The deep trench is filled with a first conducting layer. The first conducting layer and the spacer are recessed to a predetermined depth sequentially. A second barrier layer is conformally formed on the first sidewall, the sidewall layer, and the first conducting layer. The deep trench is filled with a second conducting layer.

Please replace the paragraph at page 7, line 8 with the following rewritten paragraph:

– In FIG. 3c, the deep trench 304 is ion implanted ~~to~~ at a predetermined angle by a gas mixture containing F, such as ~~chlorine~~ fluorine gas, to form an ion doped area on a first sidewall 304 and the surface of the poly layer 307. The predetermined angle is about 10 to 80°.

Please replace the paragraph at page 7, line 21 with the following rewritten paragraph:

– In FIG. 3e, a sidewall layer 309, such as p+ type epi-silicon layer, is formed on the second sidewall 304b of the top portion of the trench using the oxide layer 308 as a mask. The oxide layer 308 is then removed. A barrier layer 310, such as a silicon nitride layer, is conformally formed on the exposed semiconductor substrate 301 of the first sidewall 304a, the poly layer 307, and sidewall layer 309. The material of the sidewall layer 309 is the same as the semiconductor substrate 301.